REMARKS

Applicant notes with appreciation the finding that claims 5-7, 9-11, 17-19 and 21-23 would be allowable if rewritten in independent form. However, those claims have not been so rewritten because it is believed that the corresponding base claims should be allowed for the reasons presented below.

The objections to claims 19 and 25 have been addressed by the above claim amendments. Claims 1, 13 and 25 have also been amended to present a more consistent use of terms.

Claims 1-3, 8, 12-15, 20 and 24-25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Collins (U.S. patent 4,797,589). Claims 4 and 16 were rejected under 35 U.S.C. 103(a) as being unpatentable over Collins in view of Thomas (U.S. patent 5,761,242). Those rejections are respectfully traversed and reconsideration is requested.

As recited in claims 1, 13 and 25, the present invention relates to a digital cross connect having plural switching stages, each stage having plural switches which receive plural frames of time multiplexed input data and which switch the data in time and space. The invention relates to a method and mechanism for distributing a frame clock to all of the switches. Specifically, one of the switches, preferably a middle-stage switch, is selected as the master. The frame clock is propagated from the master to downstream switches of the plural switching stages and also from the output switches to the input switches. This propagation is illustrated in Fig. 8 where the clock first propagates from the master 54 to the switches of the output stage 50. In this embodiment, the input and output stages share chips, so the frame clock then readily propagates to the input stage. The propagation of the frame clock can be matched to data distribution between the switches as recited in claims 2 and 14 so that, as data signals are delayed, they remain properly aligned to the frame clock. A frame counter at each switch may be aligned to a defined offset from the frame clock as recited in claims 8 and 20. In particular embodiments, the frame clock may be imbedded in a frame of data as in the A1 byte of the SONET frame (claims 3-7, 15-19).

Collins refers to a master/slave arrangement of a clock in the paragraph bridging columns 2 and 3. However, there is no suggestion of how that clock is distributed from a master to the slave. In particular, there is no suggestion that the clock be propagated to downstream switches and then from output switches to input switches. More specifically, there is no suggestion of matching propagation of the frame clock to data distribution between the switches or to deriving the frame clock from a frame of data. Nor is there any suggestion of aligning a frame counter to a defined offset from the frame clock.

With respect to claims 4 and 16, which recite that the frame clock is derived from an A1 byte of a SONET frame, the Examiner has cited Thomas. Although Thomas does refer to the well known A1 and A2 framing byte of a SONET frame, there is no suggestion that those bytes be used as a mechanism for propagating a frame clock through plural switching stages.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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